ELIZADE UNIVERSITY ILARA MOKIN, ONDO STATE

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

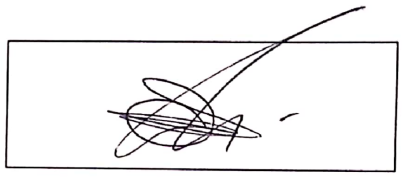
SECOND SEMESTER EXAMINATION, 2019/2020 ACADEMIC SESSION

COURSE TITLE: ELECTRONIC CIRCUIT I

COURSE CODE: EEE 321

EXAMINATION DATE:

COURSE LECTURER: DR K. O. TEMIKOTAN



HOD's Signature

TIME ALLOWED: 3 HOURS

INSTRUCTION

1. ANSWER ANY **FIVE** QUESTIONS
2. SEVERE PENALTIES APPLY FOR MISCONDUCT, CHEATING, POSSESSION OF UNAUTHORIZED MATERIALS DURING EXAM.
3. YOU ARE NOT ALLOWED TO BORROW ANY WRITING MATERIALS OR CALCULATORS DURING THE EXAMINATION.
4. SMART WATCHES OR SIMILAR DEVICES ARE NOT ALLOWED IN THE EXAMINATION VENUE.

QUESTION ONE **[12 marks]**

a. In an amplifier, the maximum voltage gain is 2000 and occurs at 2 kHz. It falls to 1414 at 10 kHz and 50 Hz. Find:

(i) Bandwidth (1 mark)

(ii) Lower cut-off frequency (1 mark)

(iii) Upper cut-off frequency (1 mark)

b. For the circuit shown in the Figure Q 1, draw

i. the DC equivalent circuit (2 marks)
ii. the AC equivalent circuit. (2 marks)
iii. What is the purpose of the capacitor C_2 in the amplifier circuit? (1 mark)
iv. If a 50 mV r.m.s. input signal is applied to the amplifier, what is the peak-to-peak output voltage? Given that g_m = 5000 µS (4 marks)

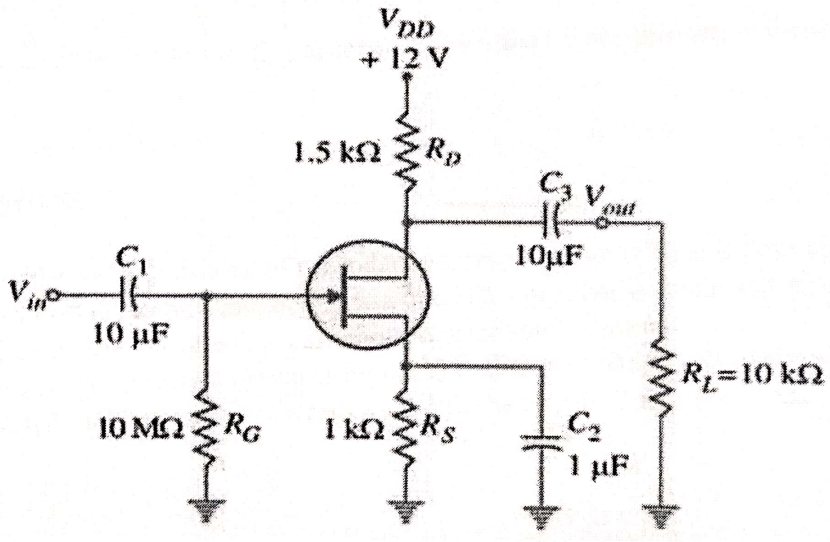


Figure Q 1

QUESTION TWO **[12 marks]**

Design a single stage common emitter amplifier given the following parameters;

V_{CC} = 12 V, I_C = 5 mA, and β (h_{fe}) = 50. Transistor (Q) = 2N3904 (silicon). State clearly the assumptions made in your design (12 marks)

QUESTION THREE **[12 marks]**

a. The Table Q 3a shows the data of an experiment on a MOSFET. If $I_{D(on)}$ = 3 mA at V_{GS} = 10V and $V_{GS(th)}$ = 3V, find the constant K for the MOSFET. (2 marks)

Table Q 3a MOSFET Data

V_{GS} (V)	I_D (mA)
5	
8	
10	
12	

b. Complete the Table Q 3a and plot the transconductance curve for the MOSFET (7 marks)

c. The following readings were obtained experimentally from a JFET:

V_{GS}	0 V	0 V	-2 V
V_{DS}	7 V	15 V	15 V
I_D	10 mA	10.25 mA	9.65 mA

Determine (i) a. c. drain resistance (ii) transconductance and (iii) amplification factor. (3 marks)

QUESTION FOUR **[12 marks]**

a. What is the main drawback of a standard common emitter (CE) amplifier circuit? (2 marks)
b. Using a neat diagram, show how a swamped CE amplifier is connected. (2 marks)
c. What is the purpose of using a swamped connection? (1 mark)
d. For the amplifier circuit shown in Figure Q 4, find the voltage gain of the amplifier with (i) C_E connected in the circuit (ii) C_E removed from the circuit. Comment on the results, (7 marks)

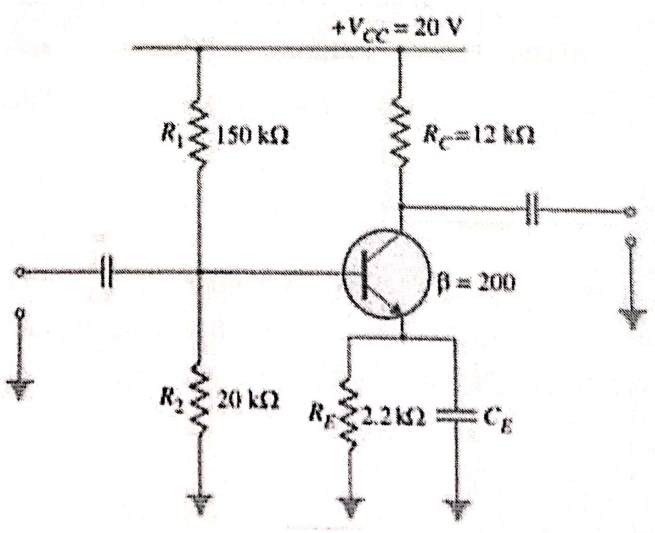


Figure Q 4

QUESTION FIVE

[12 marks]

a. In the circuit shown in Figure Q5a, $R_1 = R_2 = R_3 = R_f = 1\ k\Omega$. If $V_1 = 2V, V_2 = 1\ V, and\ V_3 = 4V$. Find V_{out}. Show all workings. (5 marks)

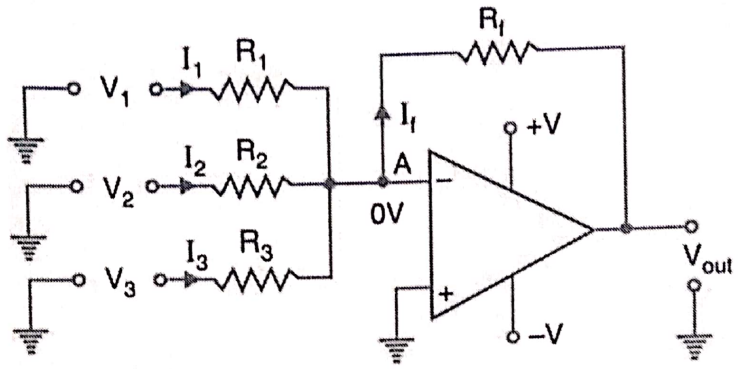


Figure Q 5a

b. A three-stage OP-AMP circuit is required to provide voltage gains of +10, – 18 and –27. Design the OP-AMP circuit. Use a 270 kΩ feedback resistor for all three circuits. What output voltage will result for an input of 150 μV? (7 marks)

QUESTION SIX

[12 marks]

a. List four methods of biasing BJTs (2 marks)

b. Given $V_{CC} = 20$ V, $R_B = 200$ kΩ, $R_C = 800$ Ω of a fixed bias CE circuit. Take $\beta = 100$

i. Draw the circuit, show the currents, and label all the components. (4 marks)

ii. Determine the value of the base current (2 marks)

iii. Determine the value of the collector current (1 mark)

iv. Determine the value of the collector-to-emitter voltage (2 marks)

v. Determine the stability factor (neglect V_{BE}) (1 mark)

QUESTION SEVEN

[12 marks]

In a transistor amplifier, when the signal changes by 0.02V, the base current changes by 10 μA and collector current by 1mA. If collector load $R_C = 5$ k Ω and $R_L = 10$ k Ω, find: (i) current gain (ii) input impedance (iii) a.c. load (iv) voltage gain (v) power gain (vi) Power gain in decibel. (12 marks)